REMARKS

Claims 1, 3-6 and 8-11 are all the claims pending in the application. Claims 1, 3-6, and 8-11 remain rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,601,176 (hereinafter, "Gibson"). Applicant submits the following in traversal.

Rejection of Claims 1, 3-6 and 8-11 under §102(e) over Gibson

Applicant submits that Gibson fails to disclose or suggest each and every element of claim 1. Specifically, Applicant submits that Gibson fails to disclose or suggest the cache controller as recited in claim 1.

Applicant emphasizes that the Examiner's characterization of the RAM 16 or the processor 14 of Gibson as corresponding to the claimed cache module is unsupportable. Nowhere in Gibson is there any mention of the RAM 16 and the processor 14 as including the claimed cache controller, tag-storing unit and data-storing unit.

Applicant's position is further supported by the Examiner's remarks in the Final Office Action which do not show that components of the RAM 16 nor components of the processor 14 correspond to the elements of the cache module, i.e., the cache controller, the tag-storing unit and the data-storing unit. Rather, the Examiner points out the operation of the separate UltraNAND device 32 as allegedly carrying out the functions recited in connection with the cache module. See page 3 of Final Office Action.

Therefore, for at least the above reasons, claim 1 is patentable.

For reasons similar to those submitted for claim 1, claims 6 and 8 are patentable.

Claims 3-5, which depend from claim 1, and claims 9-11, which depend from claim 8, are patentable for at least the reasons submitted for their respective base claims.

Applicant submits that claim 3 is additionally patentable because Gibson fails to disclose or suggest an apparatus wherein the cache controller further includes a function of extracting relevant data from the data-storing unit and transmitting the extracted data to the main control unit if the page including the designated memory address is written on the tag-storing unit, by referring to the tag-storing unit and the data-storing unit upon performing the read operation.

Applicant submits the claimed cache controller further includes a function of extracting relevant data from the data-storing unit and transmitting the extracted data to the main control unit. The extracting of the relevant data occurs if the page including the designated memory address is written on the tag-storing unit, by referring to the tag-storing unit and the data-storing unit upon performing the read operation.

Gibson, however, does not disclose or suggest having a read operation for a designated memory address and also writing the read page including the designated memory address in some sort of a tag-storing unit and the data-storing unit. Assuming arguendo, that Gibson discloses prefetching certain data, there is nothing to suggest that the prefetching is performed in the context of a read operation.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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